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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,539	09/29/2003	Frank A. Baiocchi	1-1-36-5	1844

8933 7590 02/16/2006

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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,539	BAIOCCHI ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/20/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *26-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

DETAILED ACTION

In Amendment dated 6/20/2005, Claims 6 and 23 have been amended. Claims 26-34 are newly added. This is a new ground of rejection.

Oath/Declaration

The oath/declaration filed on 9/29/2003 is acceptable.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 9/29/2003 and 6/20/2005 has/have been considered and made of record. The references cited on the PTOL 1449 form have been considered.

Drawings

The drawings are objected to for the following reason:

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Set of claims 1- 18

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 18 are rejected under 35 USC 102 (e) as being anticipated by D'Anna et al. (2003/0218209).

D'Anna et al. teaches a metal-oxide-semiconductor (MOS) device (specially refer to figs. 3-5 and related texts), comprising:

a semiconductor layer 56 of a first conductivity type (P type);

a first source/drain region 74 of a second conductivity type (N type) formed in the semiconductor layer;

a second source/drain region 63 (N type) of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region 74 ;

a gate 60 formed proximate an upper surface of the semiconductor layer 56 and at least partially between the first and second source/drain regions; and

at least one contact , the at least one contact "76" comprising:

a silicide layer "76" { (i) in para [0010]} and [0015] formed on and in electrical connection with at least a portion of the first source/drain region 74, the silicide layer extending laterally away from the gate 60 ; and

at least one insulating layer formed directly on the silicide layer [0081].

Regarding claim 2, wherein the first source/drain region comprises an n-type region 74 and a p-type region 70, and wherein the silicide layer "76" { (i) in para [0010]} is formed substantially proximate the n-type and p-type regions such that the silicide layer [0015] forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

Regarding claim 3, wherein substantially all current associated with the first source/drain region 74 passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer (fig. 3) and [0015].

Regarding claim 4, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer [0081] and {(h) of [0010]}.

Regarding claim 5, wherein the silicide layer [0015] forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer 56 that are electrically isolated from the device.

Regarding claim 6, further comprising a shielding structure 78 [0080-0084] formed proximate the upper surface of the semiconductor layer 56 and between the gate 60 and the second source/drain region 64/66, the shielding structure being electrically connected to the first source/drain region [0084], the shielding structure being spaced laterally from the gate and being substantially non-overlapping (fig. 5) relative to the gate.

Regarding claim 7, wherein the first source/drain region comprises a source region 74 and the second source/drain region comprises a drain region 64.

Regarding claims 8-9, wherein the device comprises a diffused MOS (DMOS) device [0002], the first source/drain region comprises a source region and the second source/drain region comprises a drain region (fig. 3) and wherein the MOS device comprises a lateral DMOS (LDMOS) device.

Set of claims 19-25.

Claims 19- 25 are rejected under 35 USC 102 (e) as being anticipated by D'Anna et al. (2003/0218209).

D'Anna et al. teaches an integrated circuit (IC) device (specially refer to figs. 3-5 and related texts) comprising a plurality of metal-oxide semiconductor (MOS) devices, at least one of the MOS devices [0010] comprising:

a semiconductor layer 56 of a first conductivity (P) type;

a first source/drain region 74 of a second (N) conductivity type formed in the semiconductor layer;

a second source/drain region 64/68 of the second conductivity (N) type formed in the semiconductor layer and spaced apart from the first source/drain region 74 ;

a gate 60 formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

at least one contact [0015], the at least one contact comprising:

a silicide layer "76" formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and

at least one insulating layer [0081] formed directly on the silicide layer.

Regarding claim 20, wherein the first source/drain region comprises an n-type region 74 and a p-type region 70, and wherein the silicide layer "76" { (i) in para

[0010]} is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

Regarding claim 21, wherein substantially all current associated with the first source/drain region 74 passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer (Fig.3 and [0015].

Regarding claim 22, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer [0081] and {(h) of [0010]}.

Regarding claim 23, further comprising a shielding structure 78 [0080-0084] formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate (fig. 5).

Regarding claim 24, wherein the device [0002] comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region 74 and the second source/drain region comprises a drain region 64.

Regarding claim 25, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions [0080-0084] in the semiconductor layer 56 that are electrically isolated from the device (fig. 5).

Set of claims 26-34

Newly submitted claims 26- 34 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: for **Independent claim 26** having limitation "an implant region of the first conductivity type formed at least adjacent an upper surface of said semiconductor layer and at least laterally adjacent and contacting said first source/drain region, said implant region extending laterally in a direction opposite the second source/drain region"; for **claims 28-29** with limitations "a trench sinker electrically coupling the implant region to substrate "a trench sinker comprises an implant sinker"...

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 26- 34 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818